Technical Specifications and Register Map For

mLink LongReach LoRa Module (HCMODU0250)

Version: 1.00

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Specifications

Module specifications:

Module code:	HCMODU0199
Supply voltage (VDD):	5V via mLink interface
Supply current:	2mA (sleep), 19mA (Rx), 150mA (Tx)
Radio type:	LoRa RM95
Range:	>1 kilometre in free air
Frequency:	868 to 915MHz
Max packet size:	256 bytes
Max bitrate (nominal):	9380bps (at -118dBm sensitivity)
Interface:	4 pin male mLink 0.1” headerI2C
I2C Interface speed:	400kbits/s (fast mode)
I2C default address (HEX):	0h5F
Maximum number of modules:	5 with pullups fitted, 112 with pullups removed*
Module dimensions ex headers (LxWxH):	42mm x 22mm x 5mm

*Note the maximum number of connected modules will depend on cable lengths and power requirements of each module. Do not exceed 5 mLink modules connected in series with all pullups fitted.

Register Map

Register quick reference table

REGISTER	REG ADD	Reg Bit 7	Reg Bit 6	Reg Bit 5	Reg Bit 4	Reg Bit 3	Reg Bit 2	Reg Bit 1	Reg Bit 0
STATUS	0h00	RESERVED					BUSY	REGERR	I2CERR
I2C ADD (Def = 0h5D)	0h01	NA	I2CADD						
MODULE TYPE	0h02	0h06							
MODULE SUBTYPE	0h03	0h01							
FIRMWARE VERSION	0h04	FWMAV				FWMIV			
SLEEP	0h05	RESERVED							SLEEPEN
RESERVED	0h06 to 0h09	RESERVED							
RX AVAILABLE	0h0A	RESERVED							RXAVAIL
RX SIZE	0h0B	RXSIZE							
RX READ	0h0C	RXDATA							
LAST RX ADD	0h0D	RXADD							
TX LOAD BYTE	0h0E	TXDATA							
TX SEND DATA	0h0F	TXADD							
TX DONE	0h10	RESERVED							TXDONE
RADIO MODE	0h11	RESERVED					MODE		
FREQ REG LOW	0h12	FREQ[7:0]							
RESERVED	0h13	RESERVED							
BANDWIDTH	0h14	RESERVED				BW			
SPREAD FACTOR	0h15	RESERVED				SF			
RSSI LOW	0h16	RSSI[7:0]							
RSSI HIGH	0h17	RSSI[15:8]							
LONGREACH ENABLE	0h18	RESERVED							LRMEN
TX RESENDS	0h19	RESERVED				RESENDS			
RESEND DELAY LOW	0h20	RDELAY[7:0]							
RESEND DELAY HIGH	0h21	RDELAY[15:8]							

Status register

Register address: 0h00
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED					BUSY	REGERR	I2CERR
r					NA	rw	rw

Bits 7:4 Reserved

Bit 2 **BUSY**: Busy status
This bit is set and reset by hardware
0: Ready
1: RM95 write in progress

Bit 1 **REGERR**: Register access error
This bit is set by hardware and reset by software
0: No register access error
1: Register access error caused by attempting to access an non-existent register, writing an illegal value to a register, or writing to a read only register

Bit 0 **I2CERR**: I2C bus access error
This bit is set by hardware and reset by software
0: No I2C error
1: An I2C bus error has occurred

Writing any value to this register will clear all bits

I2C Address Register

Register address: 0h01
Default value: 0h5F

7	6	5	4	3	2	1	0
N/A	I2CADD						
r	rw						

Bit 7 N/A: Returns 0
Bits 6:0 **I2CADD**: 7 bit I2C address (default factory reset value = 0h5D)

These bits are set by software
Values written to this register will be stored in non-volatile memory
Valid address range is 0h08 to 0h77. Addresses outside this range will be ignored but will set the **REGERR** bit in the status register.

Before a new address can be written to this register it must first be unlocked by writing bytes 0x55 followed by 0xAA. The new address byte must then be written within 100ms of writing the 0xAA byte otherwise the unlock sequence will timeout and reset.

Module Type Register

Register address: 0h02
Default value: 0h06

7	6	5	4	3	2	1	0
MTYP							
r							

Bits 7:0 **MTYP**: 8 bit value representing the module type.

This register will always return 0h06, signifying this module type is ‘wireless transceiver’

Module Subtype Register

Register address: 0h03
Default value: 0h01

7	6	5	4	3	2	1	0
STYP							
r							

Bits 7:0 **STYP**: 8 bit value representing the module subtype.
This register will always return 0h01 for the LongReach wireless transceiver module.

Firmware Version Register

Register address: 0h04
Default value: 0hXX

7	6	5	4	3	2	1	0
FWMAV				FWMIV			
r				r			

Bits 7:4 **FWMAV**: 4 bit value representing the modules major firmware version
Bits 3:0 **FWMAV**: 4 bit value representing the modules minor firmware version

Sleep Register Register

Register address: 0h05
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED							SLEEPEN
w							

Bits 7:1 Reserved
Bit 0 **SLEEPEN**: Sleep enable
This bit is set by software. Writing a 1 to this bit will place the module into low power sleep mode.
1: Enable sleep mode

Sleep mode is exited (SLEEPEN = 0) automatically on the next register read or write.

Rx Data Available Register

Register address: 0h0A
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED							RXAVAIL
r							

Bits 7:1 Reserved
Bit 0 **RXAVAIL**: New Rx packet has been received
This register is set and reset by hardware.

Indicates whether a new data packet has been received where:
0 = Rx buffer empty
1 = Rx buffer contains a new Rx packet

This bit is cleared when the last byte is read from the Rx buffer.
Whilst set, any new packets received will be ignored.

Rx Size Register

Register address: 0h0B
Default value: 0h00

7	6	5	4	3	2	1	0
RXSIZE							
r							

Bits 7:0 **RXSIZE**: Size of the received packet in bytes
This register is set and reset by hardware.

Contains the size of a received packet in bytes (max 255). The register can be used to determine how many bytes will need to be read out of the RX buffer when a new packet has been received.

Notes: This register is cleared once the last byte has been read from the Rx buffer.

Rx Read Register

Register address: 0h0C
Default value: 0hFF

7	6	5	4	3	2	1	0
RXDATA							
r							

Bits 7:0 **RXDATA**: Rx data buffer

This register is set and reset by hardware.

Reading from this register will return the next byte in the Rx buffer. Data is output in a FIFO format with the fist byte in the Rx buffer being output fist.

To correctly read all the data out of the Rx buffer the following sequence should be followed:

Poll the RXAVAIL bit to determine if a new packet has been received and that the Rx buffer contains valid data.

If RXAVAIL = 1 then read the RXSIZE register to determine the size in bytes of the received packet.

Read the RXDATA register RXSIZE number of times to read the full packet out of the Rx buffer.

Notes: Once the last byte is read, further reads to this register will return 0hFF

Last Rx Add Register

Register address: 0h0D
Default value: 0h00

7	6	5	4	3	2	1	0
RXADD							
r							

Bits 7:0 **RXADD**: Address of last LongReach packet

This register is set and reset by hardware.

Reading from this register will return the address of the last received LongReach packet. To receive a LongReach packet LongReach mode must be enabled (LRMEN=1).

Tx Load Byte Register

Register address: 0h0E
Default value: NA

7	6	5	4	3	2	1	0
TXDATA							
w							

Bit 7:0 **TXDATA**: Load a byte of data into the Tx buffer.
This register is set by software.

Writing data to this register will load the data in sequence into the Tx buffer ready for transmission. When the last byte has been written it can be transmitted by enabling the TXSEND bit. Data is then transmitted in the order it was loaded into the Tx buffer.

When in normal mode (LRMEN=0) the maximum number of bytes that can be written to the Tx buffer is 255.

When in LongReach mode (LRMEN=1) the maximum number of bytes that can be written to the Tx buffer is 32.

Writing beyond the maximum buffer size will result in the data overwriting the last byte in the buffer.

Tx Send Data Register

Register address: 0h0F
Default value: NA

7	6	5	4	3	2	1	0
TXADD							
w							

Bits 7:0 **TXADD**: Triggers a transmit of the data in the Tx buffer.

This bit is set and reset by software.

For normal (LRMEN = 0) mode writing any value to this register will trigger a transmit of the data held within the Tx buffer

For LongReach mode (LRMEN = 1) writing a value to this register will trigger a transmit of the data held within the Tx buffer with the value written being used as the LongReach destination address. This value should therefore match the address of the destination module.

In both cases the TXDONE bit can be polled to determine when the module has finished transmitting the data.

Tx Done Register

Register address: 0h10
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED							TXDONE
r							

Bits 7:1 Reserved
Bit 0 **TXDONE**: Module transmit state.

This bit is set and reset by hardware.

This bit can be used to determine if the module is currently transmitting data where:

0 = module is idle/transmission is complete
1 = module is currently transmitting

Radio Mode Register

Register address: 0h11
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED					MODE		
w							

Bits 7:3 Reserved
Bits 2:0 **MODE**: Sets the radio mode.
These bits are set and reset by software.

Sets the operating mode of the radio where:
0b000 = Sleep mode
0b001 = Standby mode
0b101 = Continuous receive mode
0b110 = Single receive mode (returns to idle after receiving a packet)

Notes:

After writing to this register the BUSY bit in the status register should be polled to determine when operation has been completed. **No other register writes should be made until BUSY=0**

Frequency Low Byte Register

Register address: 0h12
Default value: 0h64

7	6	5	4	3	2	1	0
FREQ[7:0]							
w							

Bits 7:0 **FREQ[7:0]**: Sets the low byte of the radio frequency.
These bits are set and reset by software.

This register sets the low byte value for the required Tx & Rx radio frequency in MHz.

When this low byte is written to the module it will internally combine it with a fixed high byte value of 0h03. These two bytes combine to form a 10 bit value representing the required frequency.

For example, to set the module to 915MHz (393 in hex) write the lower 8 bits (0h93) to this register.

Valid frequency range is from 868 to 915 MHz. Any values written outside this range will be ignored.

Notes:

After writing to this register the BUSY bit in the status register should be polled to determine when operation has been completed. **No other register writes should be made until BUSY=0**

Bandwidth Register

Register address: 0h14
Default value: 0h07

7	6	5	4	3	2	1	0
RESERVED				BW			
w							

Bits 7:4 Reserved
Bits 3:0 **BW**: Sets the bandwidth of the radio.

These bits are set and reset by software.

Sets the bandwidth of the radio where:

0b0000 = 7.8KHz
0b0001 = 10.4KHz
0b0010 = 15.6KHz
0b0011 = 20.8KHz
0b0100 = 31.25KHz
0b0101 = 41.7KHz
0b0110 = 62.5KHz
0b0111 = 125KHz
0b1000 = 250KHz
0b1001 = 500KHz

Values outside this range will be ignored.

Notes:

After writing to this register the BUSY bit in the status register should be polled to determine when operation has been completed. **No other register writes should be made until BUSY=0**

Spread Factor Register

Register address: 0h15
Default value: 0h07

7	6	5	4	3	2	1	0
RESERVED				SF			
w							

Bits 7:4 Reserved
Bits 3:0 **SF**: Sets the spread factor of the radio.
These bits are set and reset by software.

Sets the spread factor of the radio where:

0b0110 = 64 chips/second
0b0111 = 128 chips/second
0b1000 = 256 chips/second
0b1001 = 512 chips/second
0b1010 = 1024 chips/second
0b1011 = 2048 chips/second
0b1100 = 4096 chips/second

Values outside this range will be ignored.

Notes:

After writing to this register the BUSY bit in the status register should be polled to determine when operation has been completed. **No other register writes should be made until BUSY=0**

RSSI Low Register

Register address: 0h16
Default value: 0h00

7	6	5	4	3	2	1	0
RSSI[7:0]							
r							

Bits 7:0 **RSSI[7:0]**: RSSI low byte.
This register is set by hardware.

This register, together with the RSSI high register, holds a 16 bit signed integer representing the RSSI level of the last received packet in dBm

RSSI High Register

Register address: 0h17
Default value: 0h00

7	6	5	4	3	2	1	0
RSSI[15:8]							
r							

Bits 15:8 **RSSI[15:8]**: RSSI low byte.
This register is set by hardware.

This register, together with the RSSI low register, holds a 16 bit signed integer representing the RSSI level of the last received packet in dBm

LongReach Enable Register

Register address: 0h18
Default value: 0h07

7	6	5	4	3	2	1	0
RESERVED							LRMEN
w							

Bits 7:1 Reserved
Bit 0 **LRMEN**: Enables/disables LongReach mode
These bits are set and reset by software.

Enables or disables LongReach mode where:

LRMEN = 0 Normal mode
LRMEN = 1 LongReach mode enabled

Normal mode:

In normal mode any data transmitted or received will be unmodified. Up to 256 bytes can be transmitted or received in one single packet.

This mode allows for adding your own protocol layer, encryption, addressing, etc to the data before transmitting, or just sending data in its raw format to maximise packet size.

LongReach mode:

When transmitting, data in the Tx buffer is packetised into a LongReach packet before being transmitted. Up to 32 bytes can be transmitted or received in one single packet.

When receiving, the module will receive and automatically decode LongReach packets sent by any other LongReach module and with any destination address.

This mode adds basic encryption, addressing and CRC error checking to any transmitted data and for communication to any LongReach modules.

Tx Resends Register

Register address: 0h19
Default value: 0h00

7	6	5	4	3	2	1	0
RESERVED				RESENDS			
w							

Bits 7:4 Reserved

Bits 3:0 **RESENDS**: Number of resends

These bits are set and reset by software.

Sets the number of times the module will automatically resend the contents of the Tx buffer after triggering a transmit (TXSEND = 1). Valid values a from 0 to 10 where:

0 = no resends (data is only transmitted once)
10 = 10 resends (data is transmitted 11 times)

Notes:

The module will wait for a default time of 100ms between each transmission, see RDELAY for changing this default delay time.

Values outside this range will be ignored.

Tx Resend Delay Low Register

Register address: 0h20
Default value: 0h64

7	6	5	4	3	2	1	0
RDELAY[7:0]							
w							

Bits 7:0 **RDELAY[7:0]**: Resend delay time

These bits are set and reset by software.

This register together with the Tx resend delay high register sets the wait time in ms between each resend.

Notes:

The delay time must be written to in the order of resend delay low, immediately followed by resend delay high. Valid range for the resend delay time is 100 (0.1s) to 65535 (65.535s). Any values written outside this range will be ignored.

Tx Resend Delay High Register

Register address: 0h21
Default value: 0h00

7	6	5	4	3	2	1	0
RDELAY[15:8]							
w							

Bits 7:0 **RDELAY[15:8]**: Resend delay time
These bits are set and reset by software.

This register together with the Tx resend delay low register sets the wait time in ms between each resend.

Notes:

The delay time must be written to in the order of resend delay low, immediately followed by resend delay high. Valid range for the resend delay time is 100 (0.1s) to 65535 (65.535s). Any values written outside this range will be ignored.